

## Claims

- [c1] What is claimed is:
1. An anti-fuse structure having low on-state resistance and low off-state leakage, the anti-fuse structure being set on an isolation layer of a substrate, the structure comprising:
- a silicon conductive layer set in the isolation layer, the silicon conductive layer protruding the surface of the isolation layer;
- a dielectric layer set on the top surface of the silicon conductive layer; and
- a metal conductive layer set on the surface of the isolation layer and covering the surface of the dielectric layer.
- [c2] 2. The structure of claim 1 wherein the substrate is a semiconductor wafer.
- [c3] 3. The structure of claim 1 wherein the substrate comprises a silicon-on-insulator (SOI) substrate.
- [c4] 4. The structure of claim 1 wherein the silicon conductive layer comprises doped polysilicon.
- [c5] 5. The structure of claim 1 wherein the silicon conductive layer comprises doped amorphous silicon ( $\alpha$ -Si).
- [c6] 6. The structure of claim 1 wherein the silicon conductive layer comprises doped polysilicon, doped amorphous silicon or silicide.
- [c7] 7. The structure of claim 1 wherein the silicon conductive layer further comprises a plurality of hemi-spherical grain (HSG) structures to enhance a local electric field so as to reduce an operation voltage of the anti-fuse structure.
- [c8] 8. The structure of claim 1 wherein the dielectric layer is a stacked dielectric layer stacked by at least two dielectric materials.
- [c9] 9. The structure of claim 8 wherein the dielectric layer is an ONO layer composed of a bottom oxide layer, a silicon nitride layer and a top oxide layer.

- [c10] 10. The structure of claim 1 wherein a fabrication method of the dielectric layer comprises a high temperature treatment to enhance the quality of the dielectric layer so as to reduce the off-state leakage of the anti-fuse structure.
- [c11] 11. An anti-fuse structure, the structure comprising:  
a silicon conductive layer;  
a dielectric layer set on the surface of the silicon conductive layer; and  
a metal conductive layer covering the surface of the dielectric layer.
- [c12] 12. The structure of claim 11 wherein the anti-fuse structure is set in an isolation layer positioned on a semiconductor wafer.
- [c13] 13. The structure of claim 11 wherein the anti-fuse structure is set in an isolation layer positioned on a silicon-on-insulator (SOI) substrate.
- [c14] 14. The structure of claim 11 wherein the silicon conductive layer comprises doped polysilicon.
- [c15] 15. The structure of claim 11 wherein the silicon conductive layer comprises doped amorphous silicon.
- [c16] 16. The structure of claim 11 wherein the silicon conductive layer comprises doped polysilicon, doped amorphous silicon or silicide.
- [c17] 17. The structure of claim 11 wherein a surface of the silicon conductive layer further comprises a plurality of hemi-spherical grain (HSG) structures to enhance a local electric field so as to reduce an operation voltage of the anti-fuse structure.
- [c18] 18. The structure of claim 11 wherein the dielectric layer is a stacked dielectric layer stacked by a plurality of dielectric materials.
- [c19] 19. The structure of claim 18 wherein the dielectric layer is an ONO layer.
- [c20] 20. The structure of claim 19 wherein a fabrication method of the dielectric layer comprises a high temperature treatment to enhance the quality of the dielectric layer so as to reduce the off-state leakage of the anti-fuse structure.